IN THE CLAIMS

Please amend the claims as follows.

1. (Previously Presented) An apparatus for controlling a physical layer interface of a network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program;

a random access memory capable of storing a downloadable software control program downloaded from an external processing system; and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode is capable of executing said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of executing said downloadable software control program in place of said embedded control program to thereby control said physical layer interface;

wherein said microcontroller comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address to said RAM in a first one of said plurality of control registers.

2. (Original) The apparatus as set forth in Claim 1 wherein said ROM is an internal ROM in said microcontroller.

3. (Original) The apparatus as set forth in Claim 1 wherein said RAM is an internal RAM in said microcontroller.

4. (Original) The apparatus as set forth in Claim 1 wherein said ROM is an external ROM coupled to said microcontroller.

5. (Original) The apparatus as set forth in Claim 1 wherein said RAM is an external RAM coupled to said microcontroller.

6. (Original) The apparatus as set forth in Claim 1 wherein said microcontroller downloads said downloadable software control program from said external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

7. (Original) The apparatus as set forth in Claim 6 wherein said microcontroller downloads said downloadable software control program via a medium access control (MAC) layer interface coupling said external processing system and said physical layer interface.

8. (Cancelled).

9. (Previously Presented) A processing system comprising:

a data processor;

a hard disk drive capable of storing a network interface card (NIC) configuration file containing a downloadable software control program; and

a network interface card for coupling said processing system to a data network, said network interface card comprising an apparatus for controlling a physical layer interface of said network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program;

a random access memory capable of storing a downloadable software control program downloaded from an external processing system; and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode is capable of executing said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of executing said downloadable software control program in place of said embedded control program to thereby control said physical layer interface;

wherein said microcontroller comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address to said RAM in a first one of said plurality of control registers.

10. (Original) The processing system as set forth in Claim 9 wherein said ROM is an internal ROM in said microcontroller.

11. (Original) The processing system as set forth in Claim 9 wherein said RAM is an internal RAM in said microcontroller.

12. (Original) The processing system as set forth in Claim 9 wherein said ROM is an external ROM coupled to said microcontroller.

13. (Original) The processing system as set forth in Claim 9 wherein said RAM is an external RAM coupled to said microcontroller.

14. (Original) The processing system as set forth in Claim 9 wherein said microcontroller downloads said downloadable software control program from said external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

15. (Original) The processing system as set forth in Claim 14 wherein said microcontroller downloads said downloadable software control program via a medium access control (MAC) layer interface coupling said external processing system and said physical layer interface.

16. (Cancelled).

17. (Previously Presented) For use in a network interface card having a physical layer interface controllable by a microcontroller embedded therein, a method of operating the microcontroller comprising the steps of:

in a first operating mode, executing an embedded control program stored in a read only memory (ROM) coupled to the microcontroller to thereby control the physical layer interface;

in a second operating mode, executing a software control program downloaded from an external processing system and stored in a random access memory (RAM) coupled to the microcontroller in place of the embedded control program to thereby control the physical layer interface; and

switching from the first operating mode to the second operating mode when the external processing system stores a jump address to the RAM in a first one of a plurality of control registers in the microcontroller.

18. (Original) The method as set forth in Claim 17 wherein the ROM is an internal ROM in the microcontroller.

19. (Original) The method as set forth in Claim 17 wherein the RAM is an internal RAM in the microcontroller.

20. (Original) The method as set forth in Claim 17 wherein the ROM is an external ROM coupled to the microcontroller.

21. (Original) The method as set forth in Claim 17 wherein the RAM is an external RAM coupled to the microcontroller.

22. (Original) The method as set forth in Claim 17 wherein the step of downloading comprises the step of downloading the software control program from the external processing system via a media independent clock (MDC) signal line and a media independent input/output (MDIO) signal line.

23. (Original) The method as set forth in Claim 22 wherein the step of downloading comprises the step of downloading the software control program via a medium access control (MAC) layer interface coupling the external processing system and the physical layer interface.

24. (Currently Amended) The apparatus of Claim ~~8~~ 1, wherein the first control register comprises a last register in a first register file in the microcontroller.

25. (Previously Presented) The apparatus of Claim 24, wherein the microcontroller includes 256 register files, each register file containing 32 16-bit registers.